CLAIMS:

1. Voltage level monitoring circuit, comprising:
- a first reference current source (5) for generating a first reference current (I_{ref1});
- a monitoring current source (4) for generating a monitoring current (I_M) derived from a voltage (V_M) to be measured;
- a comparator device (10) comprising a first current input (11) coupled for receiving the first reference current (I_{ref1}) and a second current input (12) coupled for receiving the monitoring current (I_M), and at least one measuring signal output (13), the comparator being arranged for comparing the currents received at its two current inputs (11, 12) and for generating at the measuring signal output (13) a measuring signal (S) with a first value when the current received at its second current input (12) is less than the current received at its first current input (11), and with a second value when the current received at its second current input is more than the current received at its first current input.

2. Voltage level monitoring circuit according to claim 1, wherein the first reference current source (5) comprises a PMOS transistor (50) having its source coupled for receiving the voltage (V_{DD}) to be measured, having its gate coupled for receiving a bias voltage (V_{bias}), and having its drain coupled to the first current input (11) of the comparator device (10).

3. Voltage level monitoring circuit according to claim 1 ~~or 2~~, further comprising a second reference current source (6) for generating a second reference current (I_{ref2}), a current output of the second reference current source (6) being coupled to the comparator device (10) through a controllable switch (7).

4. Voltage level monitoring circuit according to claim 3, wherein the controllable switch (7) is controlled by a control signal (Sc) generated by the comparator device (10).

5. Voltage level monitoring circuit according to claim 4, wherein the control signal (Sc) renders the controllable switch (7) conductive when the magnitude of the current

received at the first input (11) of the comparator device (10) is higher than the magnitude of the current received at the second input (12) of the comparator device (10), and renders the controllable switch (7) non-conductive when the magnitude of the current received at the first input (11) of the comparator device (10) is lower than the magnitude of the current received at the second input (12) of the comparator device (10).

6. Voltage level monitoring circuit according to claim 3, ~~4 or 5~~, wherein the second reference current source (6) comprises a PMOS transistor (60) having its source coupled for receiving the voltage (V_{DD}) to be measured, having its gate coupled for receiving a bias voltage (V_{bias}), and having its drain coupled to the controllable switch (7).

7. Voltage level monitoring circuit according to claim 3, ~~4, 5, or 6~~, wherein the controllable switch (7) comprises a PMOS transistor (70) having its source coupled the current output of the second reference current source (6), having its drain coupled to the first current input (11) of the comparator device (10), and having its gate coupled to a control output (14) of the comparator device (10).

8. Voltage level monitoring circuit according to claim 1, ~~2, 3, 4, 5, 6, or 7~~, wherein the comparator device (10) comprises:
a first inverter (80) having an input (81) and an output (82);
a second inverter (83) having an input (84) and an output (85);
the output (85) of the second inverter (83) being connected to the output (13) of the comparator device (10);
the input (84) of the second inverter (83) being coupled to the output (82) of the first inverter (80);
and the input (81) of the first inverter (80) being coupled to both the first and second current inputs (11; 12) of the comparator device (10).

9. Voltage level monitoring circuit according to claim 8, as far as depending on claim 7, wherein the output (82) of the first inverter (80) is coupled to the control output (14) of the comparator device (10).

10. Voltage level monitoring circuit according to claim 1, ~~2, 3, 4, 5, 6, 7, 8, or 9~~, wherein the monitoring current source (4) comprises:

a primary current source (41) for generating a primary current (I_P), a secondary current source (42) for generating the monitoring current (I_M), and a process sensitive resistor (49) connected in series with said primary current source (41).

11. Voltage level monitoring circuit according to claim 10, wherein the primary current source (41) comprises a PMOS transistor having its source connected to the voltage (V_{DD}) to be monitored, having its gate coupled for receiving a bias voltage (V_{bias}), and having its drain connected to a first terminal of the process sensitive resistor (49).

12. Voltage level monitoring circuit according to claim 10 ~~or 11~~, wherein the secondary current source (42) comprises a first NMOS transistor having its source connected to ground and its drain coupled to the second current input (12) of the comparator device (10);
a second NMOS transistor (44) having its source connected to ground and its drain connected to a resisitive block (43) of the process sensitive resistor (49);
the gates of the first and second NMOS transistors (42; 44) being connected together and to the drain of the second NMOS transistor (44).

13. Voltage level monitoring circuit according to claim 10, 11 or 12, wherein the process sensitive resistor (49) comprises a further PMOS transistor (46) having its gate terminal connected to its drain terminal in a gate/drain node and having its source terminal coupled to the current output of the primary current source (41) for receiving the primary current (I_P).

14. Voltage level monitoring circuit according to claim 13, the process sensitive resistor (49) further comprising at least one combination of two cascaded transistors (PMOS 47, NMOS 48) connected in series with said gate/drain node, a first one of said cascaded transistors (47) having its source terminal coupled to the drain terminal of the further PMOS transistor (46), a second one of said cascaded transistors (48) having drain terminal connected to the drain terminal of said first one of said cascaded transistors (47), and the gate terminals of said cascaded transistors (47, 48) being connected to each other and to the respective drain terminals of said cascaded transistors (47, 48).

15. Voltage level monitoring circuit according to any of the previous claims, wherein any of the monitoring current source (4), the first reference current source (5), and the second reference current source (6) comprises a programmable current source (90).